Preliminary

OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM66589/66P589/66Q589

OLMS-66K Series CMOS 16-Bit Microcontroller

GENERAL DESCRIPTION

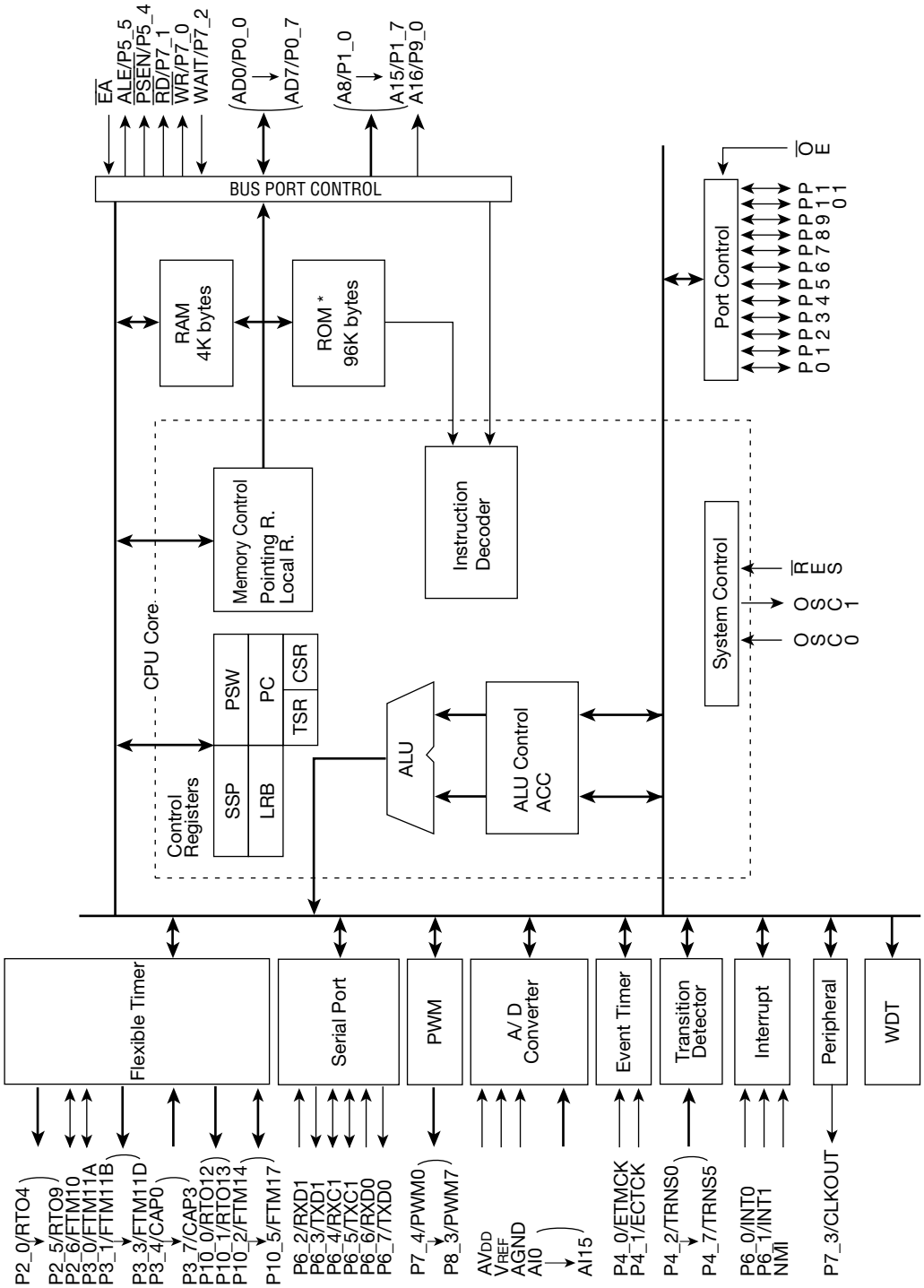
The MSM66589/66P589/66Q589 is a high-speed, high-performance 16-bit microcontroller that employs OKI original nX-8/500S CPU core.
The MSM66589/66P589/66Q589 includes a 16-bit CPU, ROM, RAM, a 10-bit A/D converter, serial ports, flexible timers, pulse-width modulator (PWM), and I/O ports.
The MSM66Q589 is a Flash EEPROM version.

FEATURES

- Program memory space : 128K bytes
  Internal ROM : 96K bytes (MSM66589/66P589)
  : 128K bytes (MSM66Q589)
- Data memory space : 64K bytes
  Internal RAM : 4K bytes
- High-speed execution
  Minimum instruction execution time : 100 nsec (@ 20 MHz)
- Built-in multiplier
- Powerful instruction set : Instruction set superior in orthogonal matrix
  8/16-bit data transfer instructions
  8/16-bit arithmetic instructions
  Multiplication and division operation instructions
  Bit manipulation instructions
  Bit logic instructions
  ROM table reference instructions
- Abundant addressing modes : Register addressing
  Page addressing
  Pointing register indirect addressing
  Stack addressing
  Immediate addressing
- I/O port
  Analog input only ports : 16 channels
  Input-output ports : 11 ports × 8 bits, 1 port × 6 bits
  (Each bit can be configured to be an input or output)
- Flexible timers
  Free run counters : 19 bits × 1, 16 bits × 1
  19-bit CAP with a divider : 4
  16-bit double buffer RTO : 6
  16-bit RTO/PWM : 2
  16-bit CAP/RTO : 6
- 8-bit general timer : 1
  8-bit event counter : 1
- 16-bit PWM : 8
  Input clock divider : 1
- 8-bit serial ports

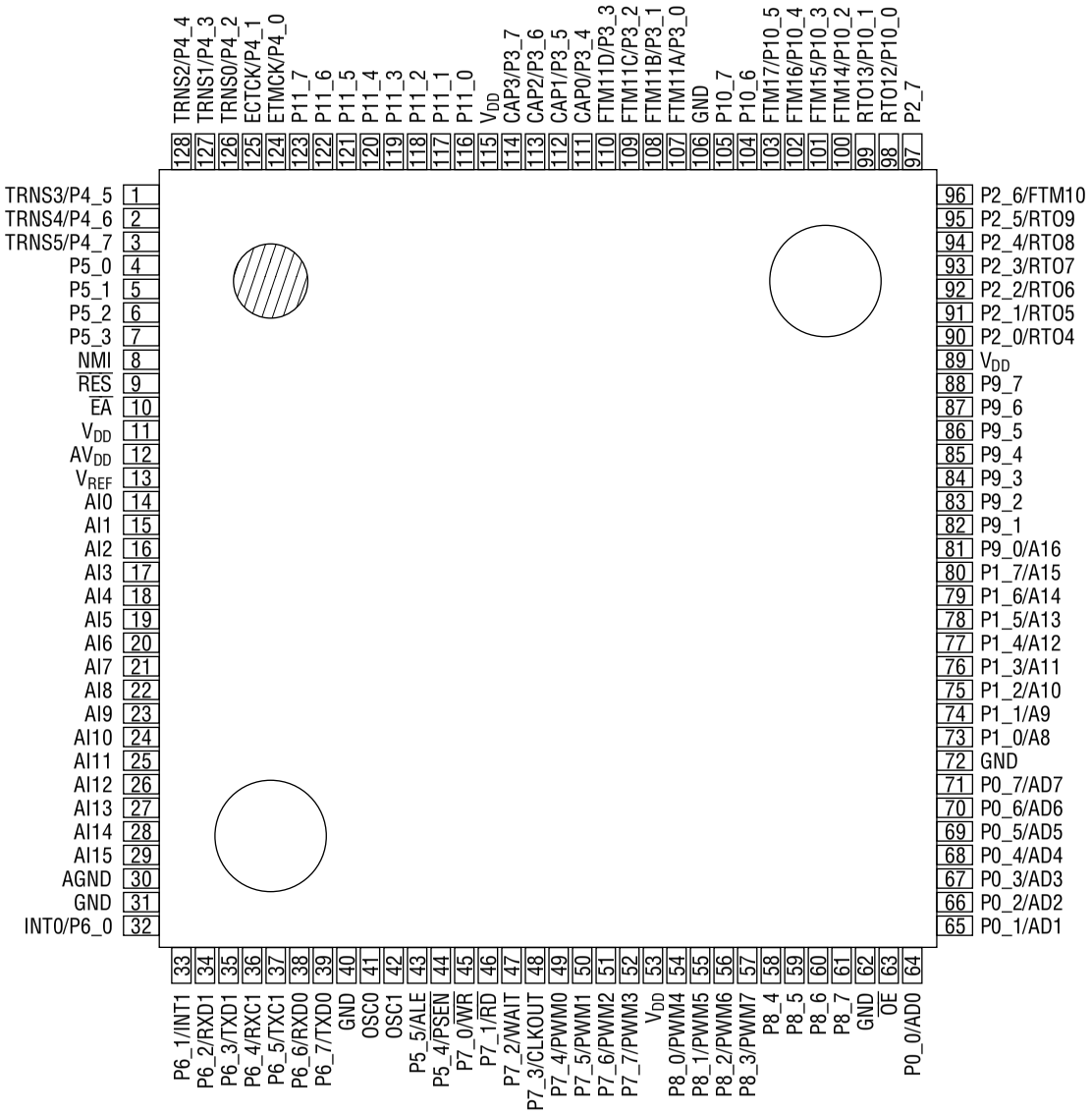
UART mode with BRG : 1
Synchronous/UART switchable mode with BRG : 1
- 10-bit A/D converter : 16 channels
- Transition detector : 6
- Watchdog timer : 1
- Interrupts
  Non-maskable : 1
  Maskable : Internal 47/external 2
  (4-level priority can be set)
- ROM window function
- Standby modes
  HALT mode
  STOP mode
- Package:
  128-pin plastic QFP (QFP128-P-2828-BK) (Product name: MSM66589-×××GS-BK)
  (Product name: MSM66P589-×××GS-BK)
  (Product name: MSM66Q589GS-BK)
  ××× indicates the code number.

BLOCK DIAGRAM



* MSM66Q589 (Flash EEPROM version) contains 128K bytes Flash EEPROM.

PIN CONFIGURATION (TOP VIEW)



128-Pin Plastic QFP (FLAT)

PIN DESCRIPTION

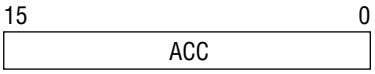
Symbol	Type	Description
P0_0-P0_7/ AD0-AD7	I/O	P0: 8-bit input-output port. Each bit can be assigned to be an input or an output. AD: When an external memory is used, these pins output the lower 8 bits of the address. These pins also input or output the data.
P1_0-P1_7/ A8-A15	I/O	P1: 8-bit input-output port. Each bit can be assigned to input or output. A: When an external memory is used, these pins output the upper 8 bits of the address.
P2_0-P2_5/ RTO4-RTO9 P2_6/FTM10 P2_7	I/O	P2: 8-bit input-output port. Each bit can be assigned to input or output. RTO: Output pin for real time output FTM10: Capture input pin or real-time output pin
P3_0-P3_3/ FTM11A-FTM11D P3_4-P3_7/ CAP0-CAP3	I/O	P3: 8-bit input-output port. Each bit can be assigned to input or output. FTM11A: Capture input pin or real-time output pin FTM11B-D: 4-port real-time output pin CAP : Capture input pin
P4_0/ETMCK P4_1/ECTCK P4_2-P4_7/ TRNS0-TRNS5	I/O	P4: 8-bit input-output port. Each bit can be assigned to input or output. ETMCK: External clock input pin of 8-bit general timer ECTCK: External clock input pin of 8-bit event counter TRNS: Transition detector input pin
P5_0-P5_3 P5_4/$\overline{\text{PSEN}}$ P5_5/ALE	I/O	P5: 6-bit input-output port. Each bit can be assigned to input or output. $\overline{\text{PSEN}}$: Strobe pulse output pin to fetch to external program memory ALE: Timing pulse output pin to latch the lower 8 bits of the address output from port 0 when the CPU accesses the external memory
P6_0/INT0 P6_1/INT1 P6_2/RXD1 P6_3/TXD1 P6_4/RXC1 P6_5/TXC1 P6_6/RXD0 P6_7/TXD0	I/O	P6: 8-bit input-output port. Each bit can be assigned to input or output. INT0, 1: External interrupt request input pin RXD1 : SCI1 Receiver data input pin TXD1 : SCI1 Transmitter data output pin RXC1 : SCI1 Receiver circuit clock pin TXC1 : SCI1 Transmitter circuit clock pin RXD0 : SCI0 Receiver data input pin TXD0 : SCI0 Transmitter data output pin
P7_0/$\overline{\text{WR}}$ P7_1/$\overline{\text{RD}}$ P7_2/WAIT P7_3/CLKOUT P7_4-P7_7/ PWM0-PWM3	I/O	P7: 8-bit input-output port. Each bit can be assigned to input or output. $\overline{\text{WR}}$: Write strobe output pin for external data memory $\overline{\text{RD}}$: Read strobe output pin for external data memory WAIT: CPU wait request input pin when accessing external data memory CLKOUT: Output pin to output clock pulse specified by PRPHF PWM: PWM output pin
P8_0-P8_3/ PWM4-PWM7 P8_4-P8_7	I/O	P8: 8-bit input-output port. Each bit can be assigned to input or output. PWM: PWM output pin
P9_0/A16 P9_1-P9_7	I/O	P9: 8-bit input-output port. Each bit can be assigned to input or output. A16: When an external program memory is used, this pin outputs the MSB of the address.
P10_0-P10_1/ RTO12-RTO13 P10_2-P10_5/ FTM14-FTM17 P10_6-P10_7	I/O	P10: 8-bit input-output port. Each bit can be assigned to input or output. RTO: Output pin for real time output. FTM: Capture input pin or real-time output pin
P11_0-P11_7	I/O	P11: 8-bit input-output port. Each bit can be assigned to input or output.

PIN DESCRIPTION (Continued)

Symbol	Type	Description
AI0-AI15	I	Analog signal input pin for A/D converter
AV_{DD}	I	Power supply input pin for A/D converter
V_{REF}	I	Reference voltage input pin for A/D converter
AGND	I	GND input pin for A/D converter
OSC0	I	Basic clock oscillation pin
OSC1	0	
$\overline{OE}$	I	When P0, P1, P2, P7_4-P7_7, and P8-P11 are in an output state and $\overline{OE}$ pin is "H" level, P0, P1, P2, P7_4-P7_7, and P8-P11 go to a high-impedance state. When P0, P1, P2, P7_4-P7_7, and P8-P11 are in an output state and $\overline{OE}$ pin is "L" level, P0, P1, P2, P7_4-P7_7, and P8-P11 output "H" or "L" level. However, when P0, P1, P2, P7_4-P7_7, and P8-P11 are in an input state, these ports are not under the influence of $\overline{OE}$ pin.
NMI	I	Nonmaskable interrupt request input pin
$\overline{RES}$	I	Low-active RESET input pin
$\overline{EA}$	I	Normally set to "H" level. If set to "L" level, the program memory goes into external access mode and accesses external program memory
V_{DD}	I	Power supply pin
GND	I	Ground pin

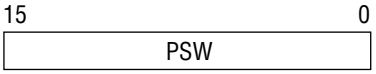
REGISTERS

Accumulator

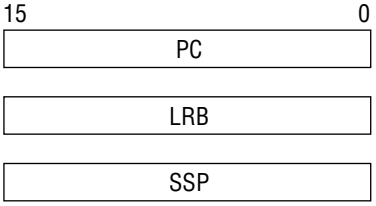


Control Register (CR)

Program Status Word



Bit 15 : Carry flag (CY)
Bit 14 : Zero flag (ZF)
Bit 13 : Half carry flag (HC)
Bit 12 : Data descriptor (DD)
Bit 11 : Sign flag (S)
Bit 10 : Master interrupt priority flag (MIP)
Bit 9 : Overflow flag (OV)
Bit 8 : Master interrupt enable flag (MIE)
Bit 7 : Multiply and accumulate operation bank flag (MAB)*
Bit 6 : User flag (F1)
Bit 5 : Bank common base (BCB1)*
Bit 4 : Bank common base (BCB0)*
Bit 3 : User flag (F0)
Bit 2-0 : System control base 2-0 (SCB2-0)
* Bit 7 (MAB), Bit 5 (BCB1), and Bit 4 (BCB0) can be used as the User flag.

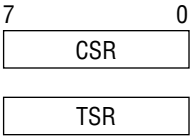


Program Counter

Local Register Base

System Stack Pointer

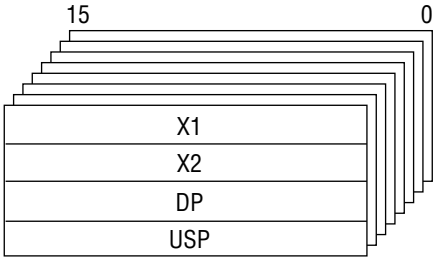
Segment Register



Code Segment Register

Table Segment Register

Pointing Register (PR)



Index Register 1
Index Register 2
Data pointer
User Stack Pointer

Local Register

	7 0	7 0
ER0	R1	R0
ER1	R3	R2
ER2	R5	R4
ER3	R7	R6

SFR

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0000	System Stack Pointer	—	SSP	R/W	16	FFFF
0001						
0002	Local Register Base	LRBL	LRB		8/16	Undefined
0003		LRBH				
0004	Program Status Word	PSWL	PSW			00
0005		PSWH				00
0006	Accumulator	ACCL	ACC			00
0007		ACCH				00
0008☆	Table Segment Register	TSR	—		8	00
0009						
000A						
000B	ROM Window Register	ROMWIN	—	R/W	8	00
000C☆	ROM Ready Control Register	ROMRDY	—			FF
000D☆	RAM Ready Control Register	RAMRDY	—			FF
000E	Stop Code Acceptor	STPACP	—	W		"0"
000F☆	Standby Control Register	SBYCON	—	R/W		C8
0010	Port 0 Data Register	P0	P0P1		8/16	00
0011	Port 1 Data Register	P1				00
0012	Port 2 Data Register	P2	P2P3			00
0013	Port 3 Data Register	P3				00
0014	Port 4 Data Register	P4	P4P5			00
0015☆	Port 5 Data Register	P5				C0
0016	Port 6 Data Register	P6	P6P7			00
0017	Port 7 Data Register	P7				00
0018	Port 0 Mode Register	P0IO	P0P1IO			00
0019	Port 1 Mode Register	P1IO				00
001A	Port 2 Mode Register	P2IO	P2P3IO			00
001B	Port 3 Mode Register	P3IO				00
001C	Port 4 Mode Register	P4IO	P4P5IO			00
001D☆	Port 5 Mode Register	P5IO				C0
001E	Port 6 Mode Register	P6IO	P6P7IO			00
001F	Port 7 Mode Register	P7IO				00
0020	Port 8 Data Register	P8	P8P9			00
0021	Port 9 Data Register	P9				00
0022	Port 10 Data Register	P10	P10P11			00
0023	Port 11 Data Register	P11				00
0024	TRNS Control Register	—	TRNSCON		16	F000
0025☆		—				
0026☆	Transition Detector	TRNSIT	—		8	C0
0027	Watchdog Timer	WDT	—	W		Stop

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0028	Port 8 Mode Register	P8IO	P8P9IO	R/W	8/16	00
0029	Port 9 Mode Register	P9IO				00
002A	Port 10 Mode Register	P10IO	P10P11IO			00
002B	Port 11 Mode Register	P11IO				00
002C☆	A/D Interrupt Control Register	ADINTCON	—		8	C0
002D☆	A/D Hardware Select Enable Register	ADHENCON	—			F0
002E	A/D Hardware Select Register	—	ADHSEL		16	0000
002F		—				
0030						
0031	Port 1 Secondary Function Control Register	P1SF	—	R/W	8	00
0032☆	Port 2 Secondary Function Control Register	P2SF	—			80
0033	Port 3 Secondary Function Control Register	P3SF	—			00
0034	Port 4 Secondary Function Control Register	P4SF	—			00
0035☆	Port 5 Secondary Function Control Register	P5SF	—			CF
0036	Port 6 Secondary Function Control Register	P6SF	—			00
0037	Port 7 Secondary Function Control Register	P7SF	—			00
0038☆	Port 8 Secondary Function Control Register	P8SF	—			F0
0039☆	Port 9 Secondary Function Control Register	P9SF	—			00
003A☆	Port 10 Secondary Function Control Register	P10SF	—			00
003B						
003C	Interrupt Request Flag Disable Register 0	IRQD0L	IRQD0	R/W	8/16	00
003D		IRQD0H				00
003E	Interrupt Request Flag Disable Register1	IRQD1L	IRQD1			00
003F		IRQD1H				00
0040	Interrupt Request Register 0	IRQ0L	IRQ0			00
0041		IRQ0H				00
0042	Interrupt Request Register 1	IRQ1L	IRQ1			00
0043		IRQ1H				00
0044	Interrupt Enable Register 0	IE0L	IE0			00
0045		IE0H				00
0046	Interrupt Enable Register 1	IE1L	IE1			00
0047		IE1H				00
0048	Interrupt Priority Control Register 00	IP00L	IP00			00
0049		IP00H				00
004A	Interrupt Priority Control Register 01	IP01L	IP01			00
004B		IP01H				00
004C	Interrupt Priority Control Register 10	IP10L	IP10			00
004D		IP10H				00
004E	Interrupt Priority Control Register 11	IP11L	IP11			00
004F		IP11H				00

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0050	PWM Counter 0	—	PWC0	R	16	FFFF
0051						
0052	PWM Counter 1	—	PWC1			FFFF
0053						
0054	PWM Counter 2	—	PWC2			FFFF
0055						
0056	PWM Counter 3	—	PWC3			FFFF
0057						
0058	PWM Counter 4	—	PWC4			FFFF
0059						
005A	PWM Counter 5	—	PWC5			FFFF
005B						
005C	PWM Counter 6	—	PWC6			FFFF
005D						
005E	PWM Counter 7	—	PWC7			FFFF
005F						
0060	PWC0 Buffer Register	—	PWC0BF	R/W		FFFF
0061						
0062	PWC1 Buffer Register	—	PWC1BF			FFFF
0063						
0064	PWC2 Buffer Register	—	PWC2BF			FFFF
0065						
0066	PWC3 Buffer Register	—	PWC3BF			FFFF
0067						
0068	PWC4 Buffer Register	—	PWC4BF			FFFF
0069						
006A	PWC5 Buffer Register	—	PWC5BF			FFFF
006B						
006C	PWC6 Buffer Register	—	PWC6BF			FFFF
006D						
006E	PWC7 Buffer Register	—	PWC7BF			FFFF
006F						
0070	PWR0 Buffer Register	—	PW0BF			0000
0071						
0072	PWR1 Buffer Register	—	PW1BF			0000
0073						
0074	PWR2 Buffer Register	—	PW2BF			0000
0075						
0076	PWR3 Buffer Register	—	PW3BF			0000
0077						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0078	PWR4 Buffer Register	—	PW4BF	R/W	16	0000
0079						
007A	PWR5 Buffer Register	—	PW5BF			0000
007B						
007C	PWR6 Buffer Register	—	PW6BF			0000
007D						
007E	PWR7 Buffer Register	—	PW7BF			0000
007F						
0080	Timer Register 0	—	TMR0	R		Undefined
0081						
0082	Timer Register 1	—	TMR1			Undefined
0083						
0084	Timer Register 2	—	TMR2			Undefined
0085						
0086	Timer Register 3	—	TMR3			Undefined
0087						
0088	Timer Register 4	—	TMR4	R/W		0000
0089						
008A	Timer Register 5	—	TMR5			0000
008B						
008C	Timer Register 6	—	TMR6			0000
008D						
008E	Timer Register 7	—	TMR7			0000
008F						
0090	Timer Register 8	—	TMR8			0000
0091						
0092	Timer Register 9	—	TMR9			0000
0093						
0094	Timer Register 10	—	TMR10			0000
0095						
0096	Timer Register 11	—	TMR11			0000
0097						
0098	Timer Register 12	—	TMR12			0000
0099						
009A	Timer Register 13	—	TMR13			0000
009B						
009C	Timer Register 14	—	TMR14			0000
009D						
009E	Timer Register 15	—	TMR15			0000
009F						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
00A0	Timer Register 16	—	TMR16	R/W	16	0000
00A1						
00A2	Timer Register 17	—	TMR17			0000
00A3						
00A4	TMR4 Buffer Register	—	TMR4BF			0000
00A5						
00A6	TMR5 Buffer Register	—	TMR5BF			0000
00A7						
00A8	TMR6 Buffer Register	—	TMR6BF			0000
00A9						
00AA	TMR7 Buffer Register	—	TMR7BF			0000
00AB						
00AC	TMR12 Buffer Register	—	TMR12BF			0000
00AD						
00AE	TMR13 Buffer Register	—	TMR13BF			0000
00AF						
00B0☆	RTO Control Register 0	RTOCON0	—		8	F8
00B1☆	RTO Control Register 1	RTOCON1	—			F8
00B2☆	RTO Control Register 2	RTOCON2	—			F8
00B3☆	RTO Control Register 3	RTOCON3	—			F8
00B4☆	RTO Control Register 4	RTOCON4	—			FC
00B5☆	RTO Control Register 5	RTOCON5	—			FC
00B6☆	RTO Control Register 6	RTOCON6	—			F8
00B7☆	RTO Control Register 7	RTOCON7	—			F8
00B8	RTO Control Register 8	RTOCON8	—			00
00B9☆	RTO Control Register 9	RTOCON9	—			F8
00BA☆	RTO Control Register 10	RTOCON10	—			F8
00BB☆	RTO Control Register 11	RTOCON11	—			F8
00BC☆	RTO Control Register 12	RTOCON12	—			F8
00BD☆	RTO Control Register 13	RTOCON13	—			F8
00BE☆	RTO Control Register 14	RTOCON14	—			F8
00BF☆	Timer Counter 0 Low-order 3 bits	TM0L	—			1F
00C0	Timer Counter 0	—	TM0		16	0000
00C1						
00C2	Timer Counter 1	—	TM1			0000
00C3						
00C4☆	TMR0 Low-order 3 Bits	TMR0L	—	R	8	Undefined
00C5☆	TMR1 Low-order 3 Bits	TMR1L	—			Undefined
00C6☆	TMR2 Low-order 3 Bits	TMR2L	—			Undefined
00C7☆	TMR3 Low-order 3 Bits	TMR3L	—			Undefined

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
00C8☆	Event Dividing Counter 0	EVDV0	—	R/W	8	C0
00C9☆	Event Dividing Counter 1	EVDV1	—			C0
00CA☆	Event Dividing Counter 2	EVDV2	—			C0
00CB☆	Event Dividing Counter 3	EVDV3	—			C0
00CC☆	EVDV0 Buffer Register	EVDV0BF	—			C0
00CD☆	EVDV1 Buffer Register	EVDV1BF	—			C0
00CE☆	EVDV2 Buffer Register	EVDV2BF	—			C0
00CF☆	EVDV3 Buffer Register	EVDV3BF	—			C0
00D0	A/D Result Register 0	ADCR0	ADCR0W	R/W (*1)	8/16 (*1)	Undefined
00D1	A/D Result Register 1	ADCR1	ADCR1W			
00D2	A/D Result Register 2	ADCR2	ADCR2W			
00D3	A/D Result Register 3	ADCR3	ADCR3W			
00D4	A/D Result Register 4	ADCR4	ADCR4W			
00D5	A/D Result Register 5	ADCR5	ADCR5W			
00D6	A/D Result Register 6	ADCR6	ADCR6W			
00D7	A/D Result Register 7	ADCR7	ADCR7W			
00D8	A/D Result Register 8	ADCR8	ADCR8W			
00D9	A/D Result Register 9	ADCR9	ADCR9W			
00DA	A/D Result Register 10	ADCR10	ADCR10W			
00DB	A/D Result Register 11	ADCR11	ADCR11W			
00DC	A/D Result Register 12	ADCR12	ADCR12W			
00DD	A/D Result Register 13	ADCR13	ADCR13W			
00DE	A/D Result Register 14	ADCR14	ADCR14W			
00DF	A/D Result Register 15	ADCR15	ADCR15W			
00E0☆	A/D Control Register L	ADCONL	—	R/W	8	80
00E1☆	A/D Control Register H	ADCONH	—			80
00E2	Timer Control Register	TMCON	—			00
00E3☆	TM Setting Register 2	TMSEL2	—			C0
00E4	TM Setting Register	—	TMSEL		16	0000
00E5☆						
00E6	TMR Mode Register	TMRMODE	—		8	00
00E7☆	TMR Mode Register 2	TMRMODE2	—			C0
00E8	Capture Control Register	—	CAPCON		16	0000
00E9☆						
00EA	Capture Control Register 2	CAPCON2	—		8	00
00EB	PWM RUN Register	PWRUN	—			00
00EC	PWM Control Register 0	PWCON0	—			00
00ED	PWM Control Register 1	PWCON1	—			00
00EE	PWM Control Register 2	PWCON2	—			00
00EF	PWM Control Register 3	PWCON3	—			00

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
00F0	PWM Interrupt Register 0	PWINTQ0	PWINTQ	R/W	8/16	00
00F1	PWM Interrupt Register 1	PWINTQ1				00
00F2	PWM Interrupt Enable Register 0	PWINTE0	PWINTE			00
00F3	PWM Interrupt Enable Register 1	PWINTE1				00
00F4	SCI0 Transmit/Receive Buffer Register	S0BUF	—		8	Undefined
00F5	SCI0 Status Register	S0STAT	—			00
00F6	SCI1 Transmit/Receive Buffer Register	S1BUF	—			Undefined
00F7	SCI1 Status Register	S1STAT	—			00
00F8☆	General-purpose 8-bit Timer Control Register	GTMCON	—			30
00F9	8-bit Event Counter	GEVC	—			00
00FA	General-purpose 8-bit Timer Counter	GTMC	—			00
00FB	General-purpose 8-bit Timer Register	GTMR	—			00
00FC☆	Event Control Register	EVNTCONL	—			88
00FD☆		EVNTCONH	—			88
00FE	Emulator Use Area					
00FF	* Note 3					
0100	Memory Size Acceptor	MEMSACP	—	W	8	"0"
0101☆	Memory Size Control Register	MEMSCON	—	R/W		FC
0102						
0103						
0104						
0105						
0106						
0107☆	Peripheral Control Register	PRPHF	—	R/W	8	(*3)
0108☆	NMI Control Register	NMICON	—			FC or 7C
0109☆	External Interrupt Control Register	EXICON	—			00
010A						
010B						
010C						
010D						
010E						
010F						
0110	SCI0 Timer	—	S0TM	R/W	16	0000
0111						
0112☆	SCI0 Timer Control Register	S0CON	—		8	02
0113☆	SCI0 Transmit Control Register	ST0CON	—			8A
0114☆	SCI0 Receive Control Register	SR0CON	—			1A
0115						
0116						
0117						

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0118	SCI1 Timer	—	S1TM	R/W	16	0000
0119						
011A☆	SCI1 Timer Control Register	S1CON	—		8	02
011B☆	SCI1 Transmit Control Register	ST1CON	—			88
011C☆	SCI1 Receive Control Register	SR1C0N	—			08
011D						
011E☆	TBC Clock Dividing Counter	TBCKDVC	—	R	8	F0
011F☆	TBC Clock Dividing Register	TBCKDVR	—	R/W		F0
0120						
0121						
0122						
0123						
0124						
0125						
0126						
0127						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

*1 The 8/16 bit operation for the ADCR items is a special word manipulation. If a byte access is made, high-order 8 bits of the A/D Result register are accessed, and if a word access is made, the 10-bit contents of the A/D Result register are accessed.
Data can be written in the even number A/D Result registers and the odd number A/D Result registers separately.
When data is first written in the A/D Result register 0 (ADCR0), data is also written in other even number A/D Result registers at a time. When data is first written in the A/D Result register 1 (ADCR1), data is also written in other odd A/D Result registers at a time.

*2 Do not access the emulator use area.

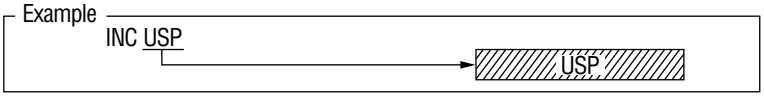
*3 The initial values of PRPHF (SFR=107H) are as follows:
At reset by $\overline{\text{RES}}$ pin: VBFF (bit 6) is "1"; CKOUT1 (bit 1) and CKOUT0 (bit 0) are "0".
At reset by WDT and BRK instructions and operation code trap: VBFF (bit 6) holds the value just before reset; CKOUT1 (bit 1) and CKOUT0 (bit 0) are "0".
In both cases, the $\overline{\text{OE}}$ pin status is read for OERD (bit 7).

ADDRESSING MODES

The MSM66589/66P589/66Q589 provides independent 64K-byte data and 128K-byte program spaces with various types of addressing modes. These modes are shown below for both RAM (for data space) and ROM (for program space).

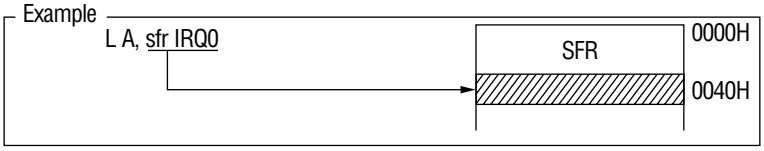
RAM Addressing Mode (for data space)

- **Register addressing**

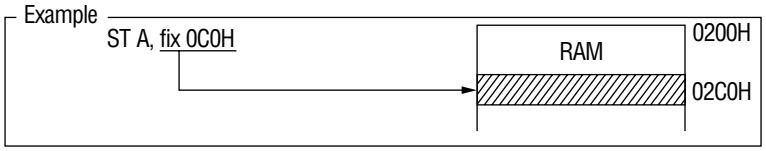


- **Page addressing**

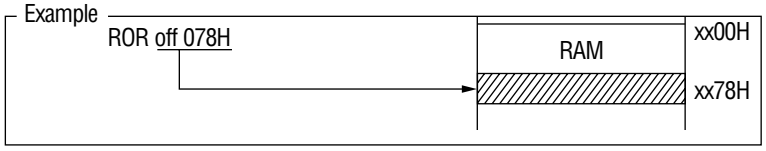
a) sfr page



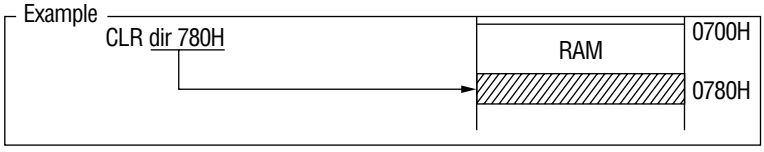
b) Fixed page



c) Current page

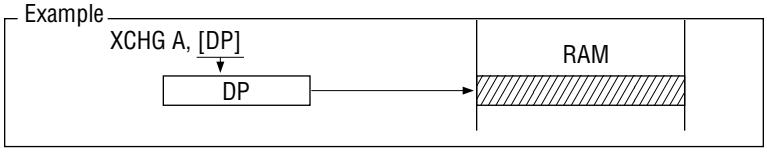


- **Direct data addressing**

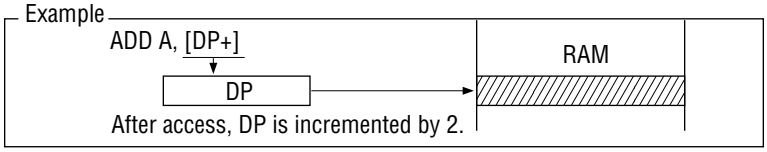


- **Pointing register indirect addressing**

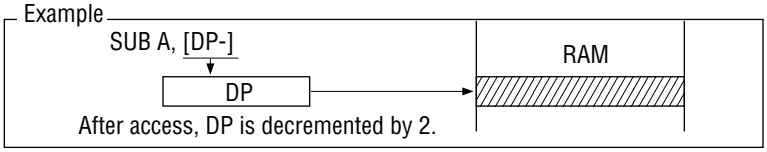
a) DP/X1 indirect



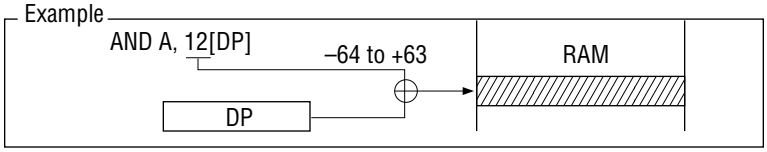
b) Post increment DP indirect



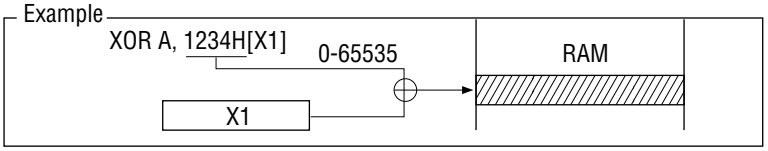
c) Post decrement DP indirect



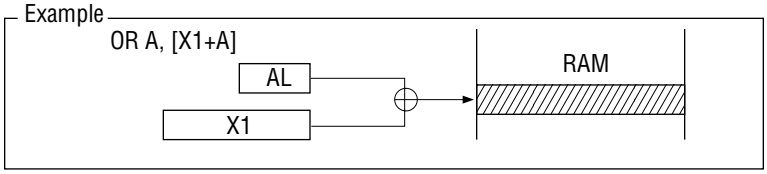
d) DP/USP indirect with 7-bit displacement



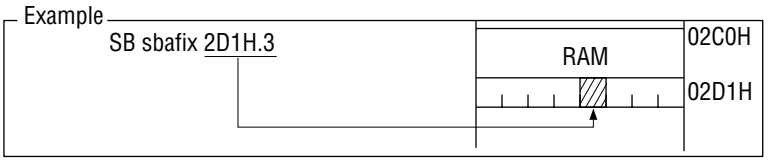
e) X1/X2 indirect with 16-bit base



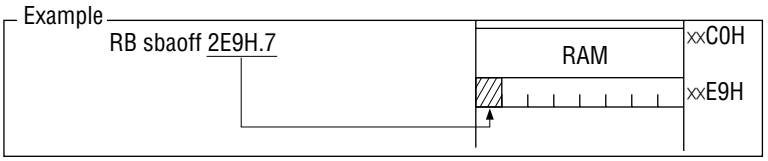
f) X1 indirect with 8-bit register (A, R0) displacement



- **Special bit area addressing**
  a) Fixed page SBA area (02C0H to 02FFH)

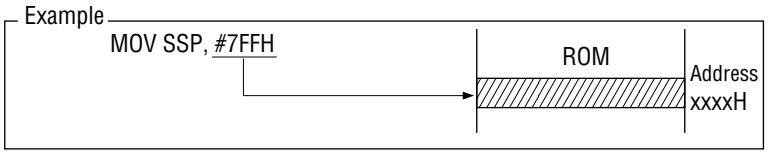


  b) Current page SBA area (××C0H to ××FFH)

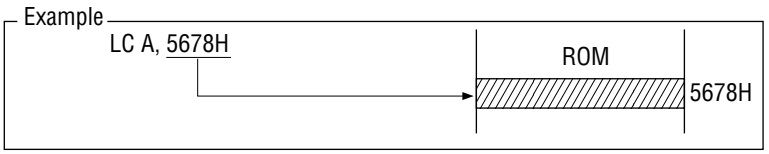


ROM Addressing Mode (for program space)

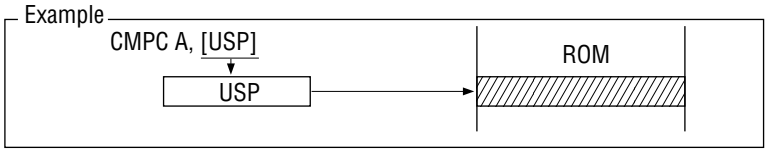
- **Immediate addressing**



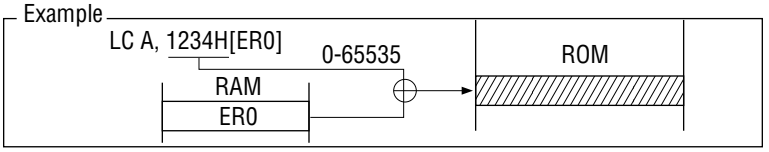
- **Table data addressing**
  TSR specifies the address segment.
  a) Direct



  b) RAM addressing indirect

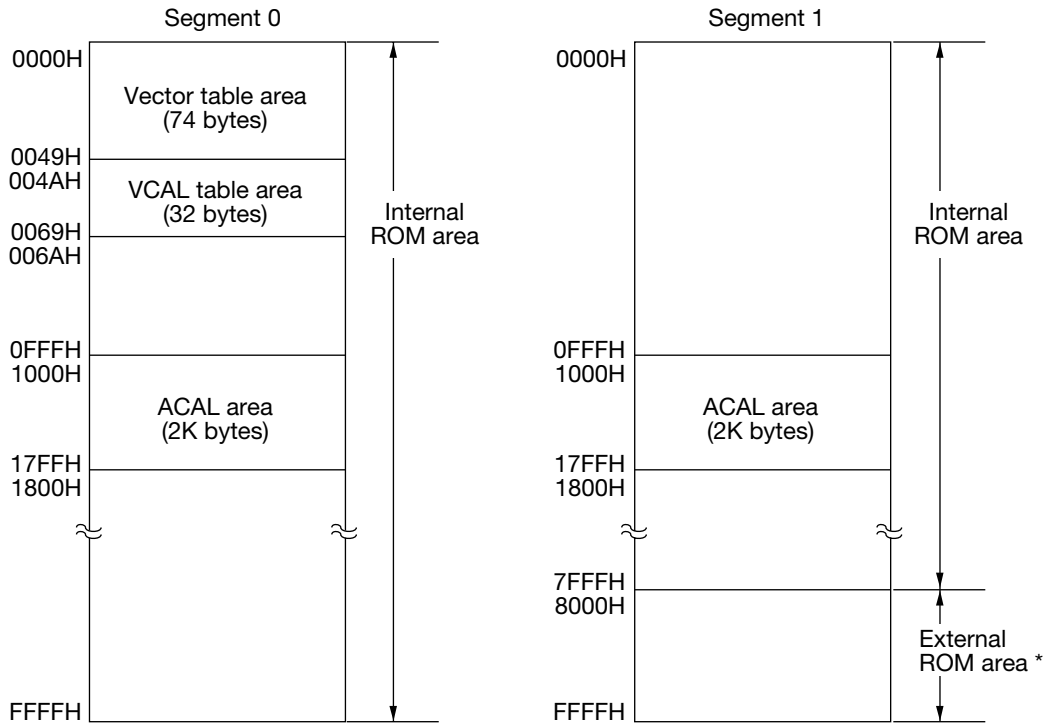


  c) RAM addressing indirect with 16-bit base



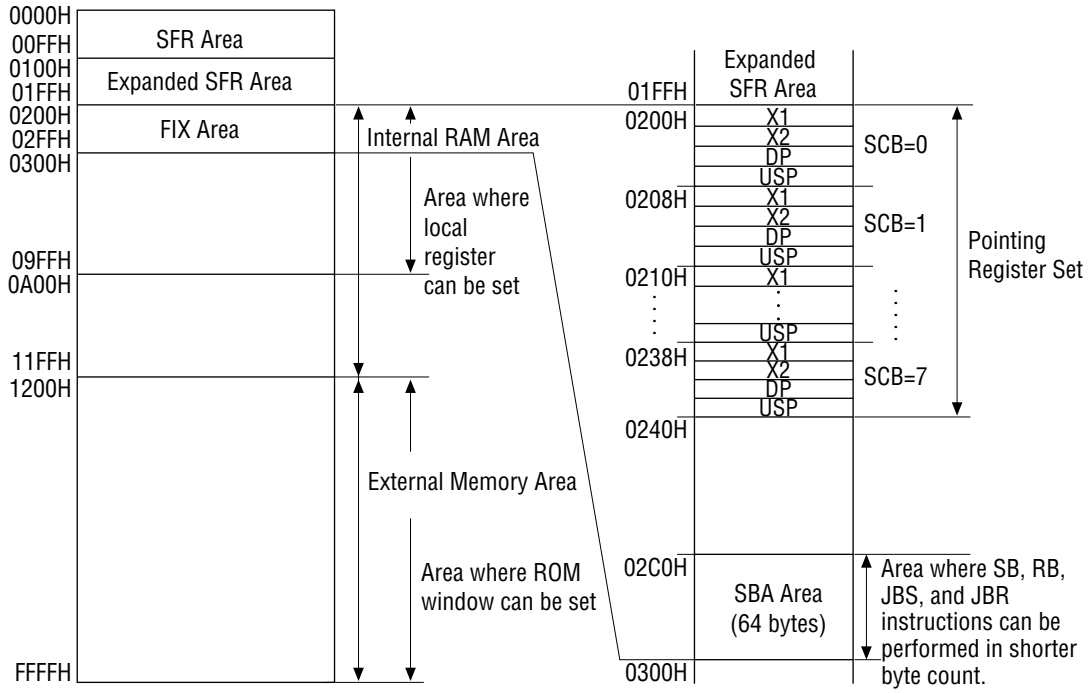
MEMORY MAP

Program Memory Space



* For MSM66Q589 (Flash EEPROM version), 8000H to 0FFFFH in Segment 1 are in the internal ROM area.

Data Memory Space



ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

Parameter	Symbol	Condition		Rating	Unit
Digital Power Supply Voltage	V_{DD}	GND=AGND=0 V Ta = 25°C		–0.3 to 7.0	V
Input Voltage	V_I			–0.3 to V_{DD}+0.3	
Output Voltage	V_O			–0.3 to V_{DD}+0.3	
Analog Power Supply Voltage	AV_{DD}			–0.3 to V_{DD}+0.3	
Analog Reference Voltage	V_{REF}			–0.3 to AV_{DD}+0.3	
Analog Input Voltage	V_{AI}			–0.3 to V_{REF}	
Power Dissipation	P_D	Ta=85°C	Per package	855	mW
			Per output	50	
Storage Temperature	T_{STG}	—		–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Digital Power Supply Voltage	V_{DD}	f_{OSC}≤20 MHz		4.5 to 5.5	V
Analog Power Supply Voltage	AV_{DD}	V_{DD}=AV_{DD}		4.5 to 5.5	
Analog Reference Voltage	V_{REF}	—		AV_{DD}–0.3 to AV_{DD}	
Analog Input Voltage	V_{AI}	—		AGND to V_{REF}	
Memory Hold Voltage	V_{DDH}	f_{OSC}=0 Hz		2.0 to 5.5	
Operating Frequency	f_{OSC}	V_{DD}=5 V±10%		0 to 20	MHz
Ambient Temperature	Ta	—		–40 to +85	°C
Fan Out	N	MOS load		20	—
		TTL load	P0, P5_4, P5_5, P7_0, P7_1	2	
			P1 to P11 (except P5_4,P5_5, P7_0, P7_1)	1	

ELECTRICAL CHARACTERISTICS

DC Characteristics (Preliminary)

(V_{DD}=5 V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
H Level Input Voltage 1	V_{IH}	–	2.2	–	V_{DD}+0.3	V
H Level Input Voltage 2, 4, 5, 6, 7			0.80V_{DD}	–	V_{DD}+0.3	
L Level Input Voltage 1	V_{IL}	–	–0.3	–	0.8	
L Level Input Voltage 2, 4, 5, 6, 7			–0.3	–	0.2V_{DD}	
H Level Output Voltage 1, 4	V_{OH}	I_{OH}=–400 µA	V_{DD}–0.4	–	–	
H Level Output Voltage 2		I_{OH}=–200 µA	V_{DD}–0.4	–	–	
L Level Output Voltage 1, 4	V_{OL}	I_{OL}=3.2 mA	–	–	0.4	
L Level Output Voltage 2		I_{OL}=1.6 mA	–	–	0.4	
Input Leakage Current 3, 6	I_{IH}/I_{IL}	V_I=V_{DD}/0 V	–	–	1/–1	µA
Input Current 5			–	–	1/–250	
Input Current 7			–	–	15/–15	
H Level Output Current 1, 4	I_{OH}	V_O=2.4 V	–2	–	–	mA
H Level Output Current 2			–1	–	–	
L Level Output Current 1, 4	I_{OL}		10	–	–	
L Level Output Current 2			5	–	–	
Output Leakage Current 1, 2, 4	I_{LO}	V_O=V_{DD}/0 V	–	–	±2	µA
Input Capacitance	C_I	f=1 MHz, Ta=25°C	–	5	–	pF
Output Capacitance	C_O		–	7	–	
Analog Reference Current	I_{REF}	A/D in operation	–	–	6	mA
		A/D stopped	–	–	10	µA
Current Consumption (in STOP mode)	I_{DDS}	V_{DD}=2 V, Ta=25°C*	–	0.2	10	µA
		*	–	1	100	
Current Consumption (in HALT mode)	I_{DDH}	f_{OSC}=20 MHz No load	–	45		mA
Current Consumption	I_{DD}		–	80		

1. Applied to P0
2. Applied to P1 to P11 (except P5_4, P5_5, P7_0, P7_1)
3. Applied to A_{IN}
4. Applied to P5_4, P5_5, P7_0, P7_1
5. Applied to $\overline{RES}$
6. Applied to $\overline{EA}$, $\overline{OE}$, NMI
7. Applied to OSC0

* Ports for input pins are V_{DD} or GND, otherwise no load.

AC Characteristics (Preliminary)

• External program memory control

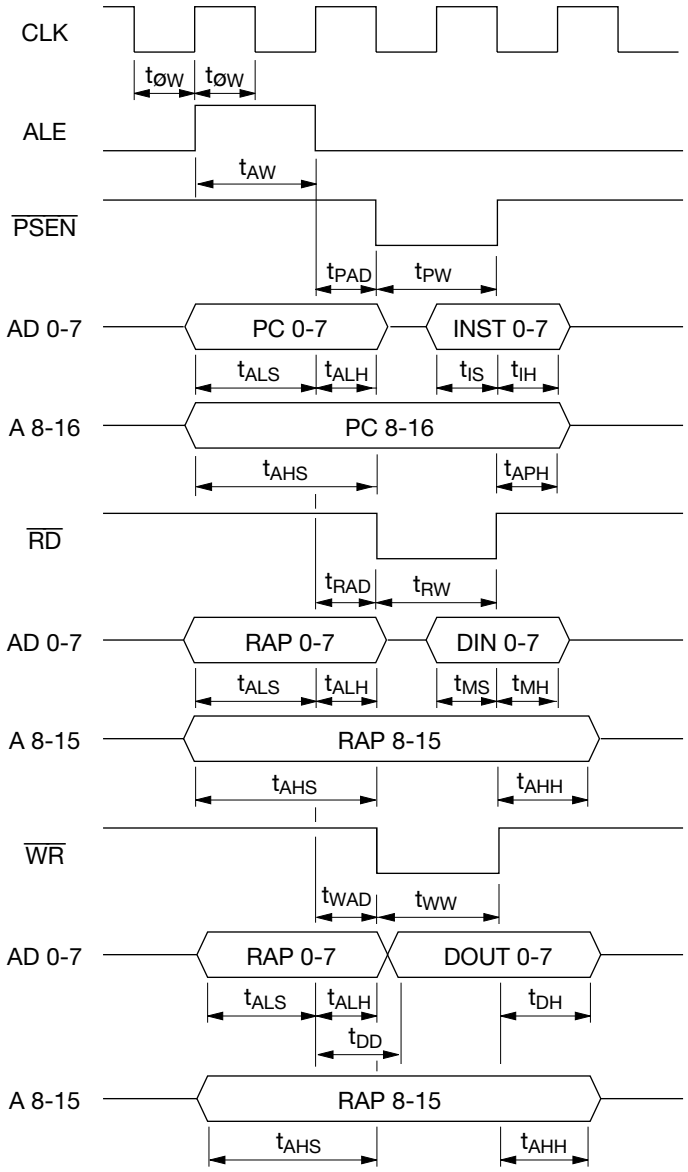
(V_{DD}=5 V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) pulse width	$t_{øW}$	—	25	—	nsec
ALE pulse width	t_{AW}	C_L=50 pF	$2t_{øW}$–10	—	
$\overline{PSEN}$ pulse width	t_{PW}		$2t_{øW}$–10	—	
$\overline{PSEN}$ pulse delay time	t_{PAD}		$t_{øW}$–10	$t_{øW}$+10	
Low-order address set-up time	t_{ALS}		$2t_{øW}$–10	$2t_{øW}$+10	
Low-order address hold time	t_{ALH}		$t_{øW}$–10	$t_{øW}$+10	
High-order address set-up time	t_{AHS}		$3t_{øW}$–10	$3t_{øW}$+10	
High-order address hold time	t_{APH}			$t_{øW}$+10	
Instruction set-up time	t_{IS}			—	
Instruction hold time	t_{IH}			$t_{øW}$–10	

• External data memory control

(V_{DD}=5 V±10%, Ta=–40 to +85°C)

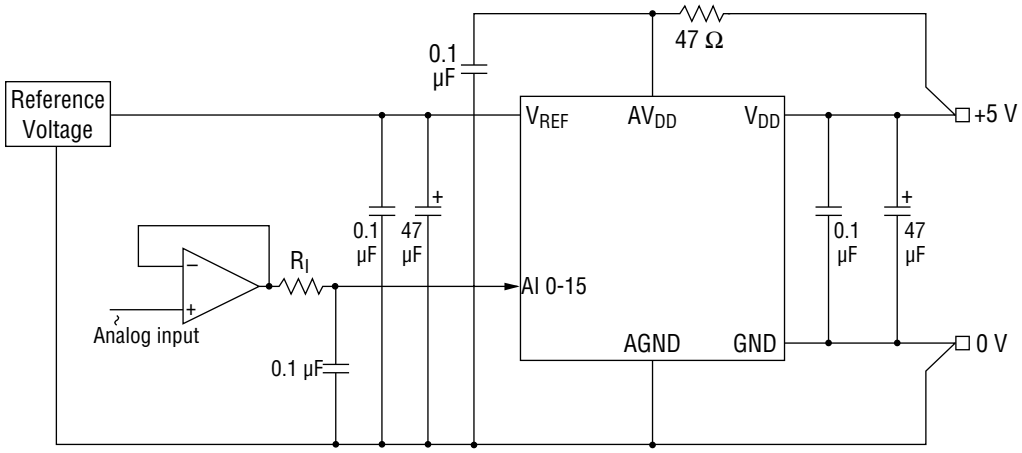
Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) pulse width	$t_{øW}$	—	25	—	nsec
ALE pulse width	t_{AW}	C_L=50 pF	$2t_{øW}$–10	—	
$\overline{RD}$ pulse width	t_{RW}		$2t_{øW}$–10	—	
$\overline{WR}$ pulse width	t_{WW}		$2t_{øW}$–10	—	
$\overline{RD}$ pulse delay time	t_{RAD}		$t_{øW}$–10	$t_{øW}$+10	
$\overline{WR}$ pulse delay time	t_{WAD}		$t_{øW}$–10	$t_{øW}$+10	
Low-order address set-up time	t_{ALS}		$2t_{øW}$–10	$2t_{øW}$+10	
Low-order address hold time	t_{ALH}		$t_{øW}$–10	$t_{øW}$+10	
High-order address set-up time	t_{AHS}		$3t_{øW}$–10	$3t_{øW}$+10	
High-order address hold time	t_{AHH}		$t_{øW}$–0	$t_{øW}$+10	
Memory data set-up time	t_{MS}			—	
Memory data hold time	t_{MH}			$t_{øW}$–10	
Data set-up time	t_{DD}		t_{ALH}–0	t_{ALH}+10	
Data hold time	t_{DH}		$t_{øW}$–10	$t_{øW}$+10	


CLK
tØW
tØW
ALE
tAW
PSEN
tPAD
tPW
AD 0-7
PC 0-7
INST 0-7
tALS
tALH
tIS
tIH
A 8-16
PC 8-16
tAHS
tAPH
RD
tRAD
tRW
AD 0-7
RAP 0-7
DIN 0-7
tALS
tALH
tMS
tMH
A 8-15
RAP 8-15
tAHS
tAHH
WR
tWAD
tWW
AD 0-7
RAP 0-7
DOUT 0-7
tALS
tALH
tDH
tDD
A 8-15
RAP 8-15
tAHS
tAHH

A/D CONVERTER CHARACTERISTICS (Preliminary)

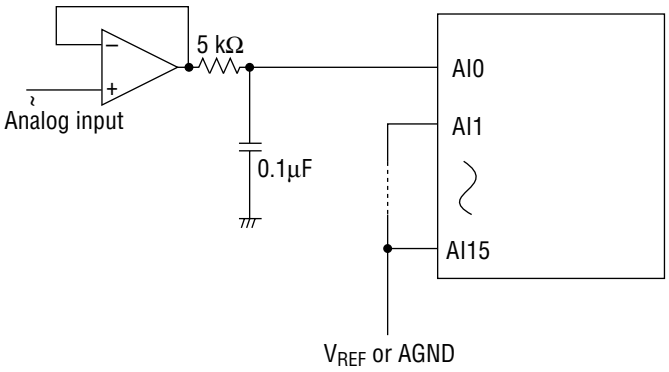
(Ta=–40 to +85°C, $AV_{DD}=V_{DD}=V_{REF}$=5 V±10%, AGND=GND=0 V, f_{OSC}=20 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to the recommended circuit. Analog input source impedance $R_I \leq 5$ kΩ t_{CONV}=19.2 µsec	—	—	10	Bit
Linearity Error	E_L		—	—		LSB
Differential Linearity Error	E_D		—	—		
Zero Scale Error	E_{ZS}			—		
Full Scale Error	E_{FS}		—	—		
Crosstalk	E_{CT}	Refer to the measuring circuit.	—	—		
Conversion Time	t_{CONV}	by ADTM set data	6.4	–	19.2	µs/CH



R_I (Analog input source impedance) ≤ 5 kΩ

Recommended Circuit



Crosstalk is defined as the difference between the A/D conversion result when applying the identical analog input to AI0 to AI15 and the A/D conversion result in the circuit in the left figure.

Crosstalk Measuring Circuit

Definitions of Terms

Resolution

The minimum distinguishable analog input value. For 10 bits, 2^{10}=1024, i.e. (V_{REF}–AGND) ÷ 1024.

Linearity error

The variance between the ideal conversion characteristics as a 10-bit A/D converter and the actual conversion characteristics. (Quantized error is therefore not included.)
In the ideal conversion, a voltage between V_{REF} and AGND is divided into 1,024 equal steps.

Differential linearity error

The smoothness of the conversion. The width of analog input voltage corresponding to the change by one bit of digital output is 1 LSB=(V_{REF}–AGND) ÷ 1024 ideally. The variance between this ideal bit size and bit size at arbitrary point in the conversion range.

Zero scale error

The variance between the ideal conversion characteristics at the switching point of digital output "000H to 001H" and actual conversion characteristics.

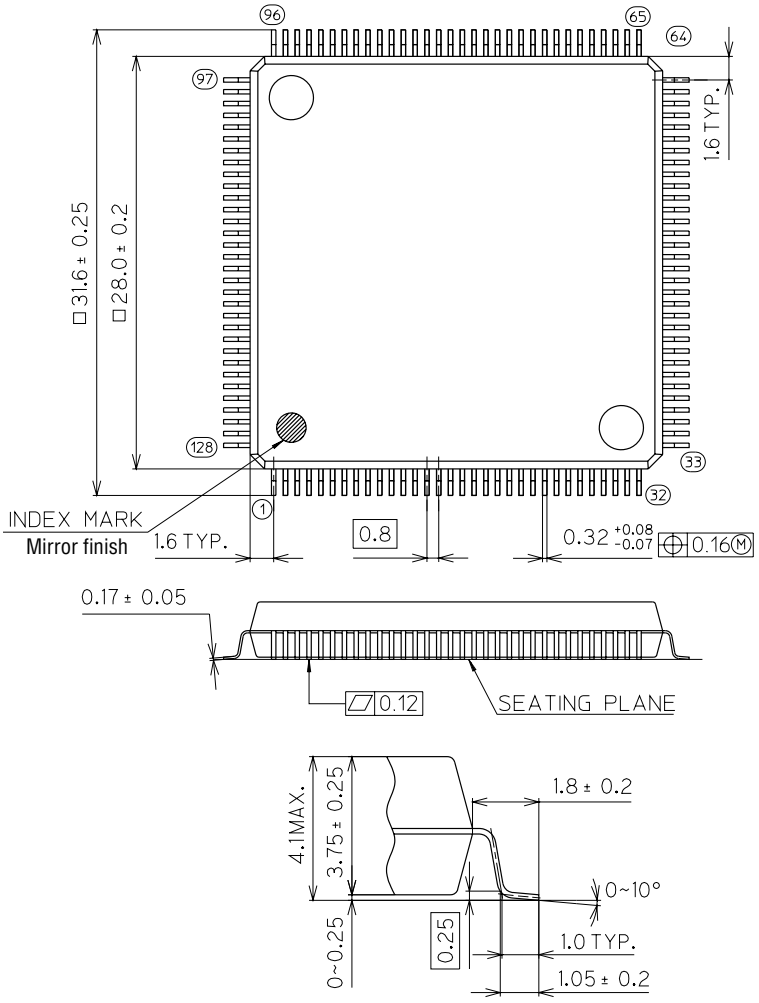
Full scale error

The variance between the ideal conversion characteristics at the switching point of digital output "3FEH to 3FFH" and actual conversion characteristics.

PACKAGE DIMENSIONS

(Unit : mm)

QFP128-P-2828-0.80-BK
QFP128-P-2828-0.80-ZK



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	5.95 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).